Reduction in the Effect of the Timing Jitter in Piezoelectric accelerometer System by Oversampling Technique

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The performance of high data rate accelerometer systems are often limited by system timing jitter. Jitter causes mismatch in the measurement of an actual value by an inaccurate sampling timing. Oversampling technique results in perfect reconstruction of bandwidth-limited signals by improving Signal-to-Noise Ratio (SNR) while avoiding aliasing as well as phase distortion by relaxing the performance of anti-aliasing filters. In this paper we demonstrate that oversampling technique can be used to reduce the side-band noise caused by timing jitter which leads to 3 dB reduction in jitter noise power for every 2x analog-to-digital converters (ADCs) sampling rate in a piezoelectric accelerometer system.

Industry 4.0 creates a smart manufacturing platform in the field of automation and data exchanging in manufacturing technologies including the Internet of things (IoT), cloud computing, and cognitive computing. Machine vibration pattern detection is an important sensor technology for monitoring the typical wear-out health parameters of the machines [2]. Piezoelectric accelerometers are widely used in condition monitoring systems to measure machinery vibration due to their excellent dynamic performance, linearity, and ease of integration in existing measurement systems. The major source of jitter is the sampling clock in high speed ADCs which are used in the application. Clock Jitter in the high data rate systems adds up undesirable noise resulting in poor performance of the accelerometer systems. The proposed Oversampling technique is achieved by eliminating some band-edge subcarriers unused, thus leading to a 3 dB reduction in jitter noise for every 2x ADCs sampling rate.

Fig. 1 presents the system level approach of a piezoelectric accelerometer system where the fully differential signal from a MEMS PZT accelerometer is connected to the charge amplifier to yield an output sensitivity of 100 mV/g which in turn is connected to the ADCs of a microcontroller system to digitize the signal, and the output is connected to the user interface software via RS232 protocol.

Fig. 2 presents the software flow of the microcontroller system to reduce the jitter noise. The frequency of interest to be studied was selected as 500 Hz. The output signal from the charge amplifier was oversampled at 8 times (8x) the Nyquist rate and was filtered and then decimated to reduce the side band jitter noise. Fig. 3 shows the measurement setup to excite the frequency of interest. The shaker was excited at an amplitude of 1 Vpp and frequency of 500 Hz, and was manually calibrated using a commercially available accelerometer. Time domain plot and Frequency domain plot were observed in custom built software.

Fig. 4 presents the time domain plot of the piezoelectric accelerometer system when excited at 1 g amplitude and 500 Hz frequency.

Fig. 5 presents the timing jitter noise of the microcontroller (MCU) clock. The clock frequency of the MCU was determined by using Timer PWM pulse which in turn was fed to an oscilloscope to analyze the timing jitter present in the MCU clock. The sources of jitter can be from thermal noise, power supply noise, ground bounce, crosstalk, and reflections [3]. Periodic clock jitter causes upper and lower jitter modulation sidebands with an offset of 250 Hz.

Fig. 6 presents the frequency domain plot of the piezoelectric accelerometer system when ADC is sampled at 1x the Nyquist rate with shaker excitation at 1 g amplitude and 500 Hz frequency. The results show the presence of side band jitter with a noise floor of -39 dB. Fig. 7 presents the frequency domain plot of the piezoelectric accelerometer system when ADC is sampled at 8x the Nyquist rate with shaker excitation at 1 g amplitude and 500 Hz frequency. The results show a noise floor of -63 dB with the reduction of side band jitters and an improvement of 24 dB in SNR. The effect of timing jitter causes a deviation of time Tn between actual sampling times and the uniform sampling intervals which can be effectively reduced using the proposed Oversampling Technique.

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Reference
**Fig. 1**: Schematic of a piezoelectric accelerometer system.

**Fig. 2**: Software flow chart of the MCU system.

**Fig. 3**: Measurement setup to verify the performance of the PZT accelerometer system.

**Fig. 4**: Time Domain Plot of 1g, 500 Hz excitation at 8x ADCs oversampling rate in the proposed PZT accelerometer system.

**Fig. 5**: Timing jitter noise in MCU clock.

**Fig. 6**: Frequency domain plot at 1x ADCs sampling rate.

**Fig. 7**: Frequency domain plot at 8x ADCs oversampling rate in the proposed PZT accelerometer system.